Amendments to the Specification

Please replace the abstract with the following amended paragraph:

A hybrid summing module is presented, wherein the summing module comprises a hyperpipelined series of multiple full-adders, half-adders, and registers. The summing module may be implemented as a Wallace tree or as a Dadda tree. The structure of the adder tree is determined by maximally partitioning bits of equal significance into groups of three to serve as inputs to full-adders. Remaining groups of two are inputs to half-adders, while remaining single bits are passed directly to registers. In one embodiment each reduction stage serves as a pipeline stage. In another embodiment the summing module is used to sum the partial products of a multiplication operation with an additional input from an accumulator in the case of multiply accumulate operations. In yet another embodiment, the summing module accelerates complex multiply operations by feeding partial products from both terms resulting in real or imaginary components into the adder tree simultaneously.

Please replace line 6 on page 3 of the specification with the following:

6. b1*c1, add to accumulator;

Please replace the paragraph beginning on line 22 of page 12 of the specification with the following paragraph:

As introduced above, certain of the terms in processing the real component are subtracted from one another. Rather than consuming a large segment of FPGA resources by implementing a subtraction module, such terms are merely ~~inverted~~ negated 402 and ~~the negative of such terms are~~ passed to the hybrid summing module 304.

Please replace the paragraph beginning on line 14 of page 16 of the specification with the following paragraph:

In accordance with the illustrated example implementation of Fig. 8, the method begins with block 802, wherein a combinatorial stage 104 of a CMAC 500 generates a plurality of partial product terms from inputs 102. As introduced above, certain ones of the partial products in a real component branch of CMAC 500 are ~~inverted~~ negated 402 before being passed to the integrated summing module 502.